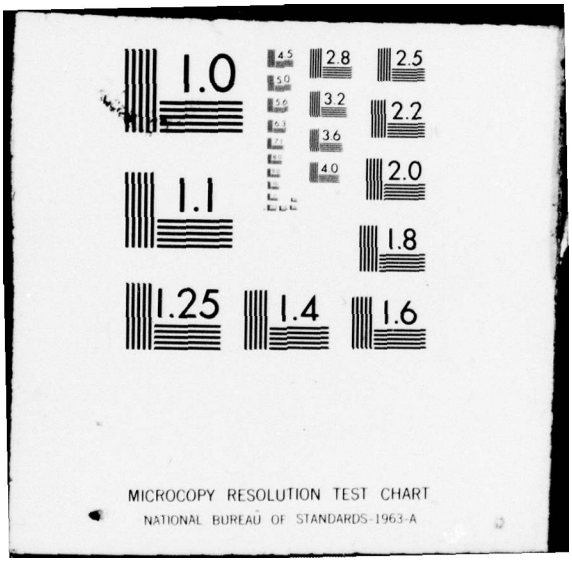
AD-A072 544 RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV F/G 9/2
MODULAR DIGITAL MISSILE GUIDANCE. (U)
NOV 78 F J LANGLEY, J DEMETRICK N00014-75-C-0549
UNCLASSIFIED BR-11013 ONR-CR233-052-5 NL

| OF |
AD
A072544

END
DATE
FILMED
9-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

REPORT ONR-CR233-052-5

AD A072544

LEVEL III

MODULAR DIGITAL MISSILE GUIDANCE

PHASE V REPORT

FRANK J. LANGLEY

JOHN DEMETRICK

Raytheon Company
Missile Systems Division
Bedford, MA 01730

Contract N00014-75-C-0549
ONR Task 233-052

30 NOVEMBER 1978

Technical Report for Period 1 Jan. 78 - 31 Oct. 78
Approved for Public Release; Distribution Unlimited

PREPARED FOR THE

OFFICE OF NAVAL RESEARCH • 800 N. QUINCY STREET • ARLINGTON • VA • 22217

NOTICES

Change of Address

Organizations receiving reports on the initial distribution list should confirm correct address. This list is located at the end of the report. Any change of address or distribution should be conveyed to the Office of Naval Research, Code 212, Washington, D.C. 22217.

Disposition

When this report is no longer needed, it may be transmitted to other authorized organizations. Do not return it to the originator or the monitoring office.

Disclaimer

The findings in this report are not to be construed as an official Department of Defense or Military Department position unless so designated by other official documents.

Reproduction

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(19) REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (17) ONR-CR233-052-5	2. GOVT ACCESSION NO. -	3. RECIPIENT'S CATALOG NUMBER -
4. TITLE (and Subtitle) (6) Modular Digital Missile Guidance, AD42466		5. TYPE OF REPORT & PERIOD COVERED Technical Report 1/1/78 to 10/31/78
		6. PERFORMING ORG. REPORT NUMBER (14) BR-11013
7. AUTHOR(s) (10) Frank J. Langley, John Demetrick		8. CONTRACT OR GRANT NUMBER(s) (15) N00014-75-C-0549
9. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Company Missile Systems Division Bedford, MA 01730		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS (11) 30 Nov 78
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research Vehicle Warfare Technology Code 212 Arlington, Virginia 22217		12. REPORT DATE 11/30/78
		13. NUMBER OF PAGES (12) 59 p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

(9) Technical Rept. 1 Jan - 31 Oct 78 on Phase 5.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Microcomputer
Microbus
Field Programmable Logic Arrays
Missile Guidance
Modular Systems
Standard Electronic Modules
Very Large Scale Integrated Circuits

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The rapidly developing microprocessor technology poses serious standardization problems for the user, particularly the military, where logistics support costs are significant over the life cycle of tactical systems. Whereas standard interface busses are now in existence e.g. (S-100, Intel Multibus, National Microbus, Motorola Microbus, European "MUBUS"), no two busses are the same.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Over 297620

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

To provide freedom of choice in microcomputer components throughout a system life cycle, a programmable microbus interface module (MIM) using common programmable control elements (PCEs), such as that described in this report, absorbs the interface irregularities of commercial microprocessors, memory and input-output (I/O) modules, thereby allowing the selection of components based on performance, support software, cost and other driving factors. Further, having made the choice of microprocessor (μP) for a given application, the user need not feel committed for all time should, for example, the requirements grow to exceed the capabilities of the processor or a more desirable μP appear on the market at a later date. The same rationale applies to I/O devices such as A-D and D-A convertors, MIL-STD-1553A/B serial interface units and others which are continually undergoing competitive improvement.

To validate the concept, a breadboard model of the MIM was designed, fabricated and tested, using high-speed field programmable logic arrays and read only memories. The results show that the MIM provides a very effective means of interfacing standard industry μc components with a simple, memory-oriented, microbus, of the form identified in earlier study phases and presented at the Annual IEEE Microcomputer Workshop in June 1976.

PREFACE

This technical report covers the work performed under Contract No. N00014-75-C-0549 from 1 January 1978 through 31 October 1978. The first draft was submitted by the authors in the form of a paper for the IEEE Computer Society "Computer" magazine on 6 December, 1978.

The purpose of this contract together with the work performed in the previous phases, was to provide the means of achieving improved performance, modularity and flexibility in the design of next generation microcomputer-based missile guidance and control systems.

Cdr. L. E. "Mac" McCullough and L/Cdr. W. Savage, Office of Naval Research Arlington, VA, were the Navy Scientific Officers.

Mr. F. J. Langley was the Principal Investigator for Raytheon and Mr. J. Demetrick was the Senior Design Engineer.

Publication of this report does not constitute Navy approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

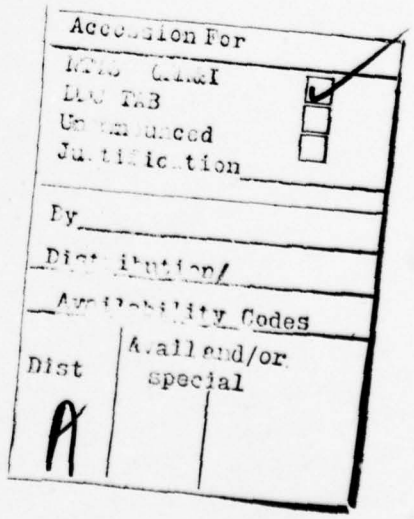


TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

Once a microprocessor is chosen for a given application, the memory and input-output interface modules/boards must conform to the interface standards associated with that processor, e.g. Intel Multibus, S-100 Bus, National Microbus; Motorola Microbus, etc. Should the system require updating at some future date the replacement of the microprocessor and associated support modules/boards with improved versions from other sources results in a complete redesign of the interface circuits.

One solution to the above, however, is a high-speed programmable interface capable of interfacing virtually any standard-product microprocessor, memory and I/O module to a simple memory-oriented microbus.

This report describes a programmable microbus interface module (MIM), which isolates the perturbations of different microprocessor interfaces from the memory and I/O circuits, such that different microprocessors can be interchanged without upset to the computer design. The work, which uses high-speed programmable logic array (PLA) techniques, is an outgrowth of the standard microbus described at the inaugural Navy/IEEE Microcomputer Standardization Workshop held at NADC, Warminster, in June 1976 (Ref. 4).

1.1 Background

Five years ago the Office of Naval Research became concerned with the inherent drawbacks of analog missile guidance and control (G&C) systems, namely; rigid/inflexible designs, limited performance and poor component commonality. To take advantage of the new trends in digital technology e.g. microprocessors and digital signal processing, a study program was initiated to analyze the functional characteristics of the entire range of air-to-air missile G&C systems and determine the computer design requirements.[1-5] Throughout the study strong emphasis was placed on modularity, in hardware and software, to enable systems to be readily updated to meet changing threat situations and to take advantage of device technology improvements without the need for major redesign.

At the system level, distributed processing was found to support the design goal and to enforce it, in the case of software, placing hardware interfaces between major system functions. Computer throughput requirements, on a major function basis, ranged from approximately 1 million operations per second (1 Mops) for guidance command generation to a few thousand operations per second for warhead fuzing and telemetry. Figure 1 shows a distributed microcomputer guidance and control system using four microcomputers interconnected via a MIL-STD-1553A/B-compatible serial digital interface. Target seeker signal processing is performed by a 16-bit processor, and separate 8-bit processors are used for gimballed-platform control, warhead fuzing and the autopilot. To satisfy the range of throughputs and system input-output (I/O) interfaces, while maintaining a high degree of component modularity and commonality, a family of fourteen microcomputer modules was defined (Fig. 2) using standard-industry microcomputer circuits

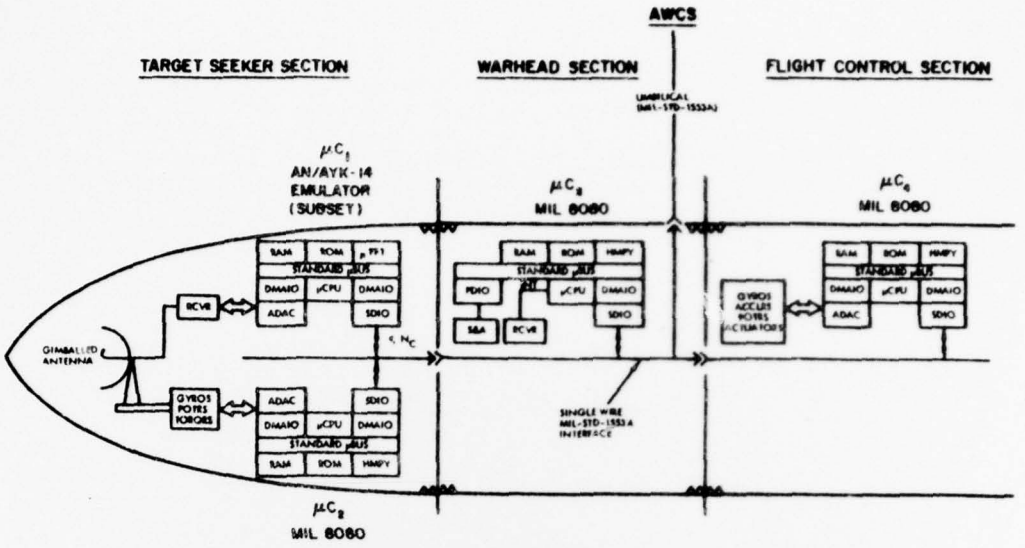


Figure 1 - Distributed Microcomputer Missile Guidance and Control System

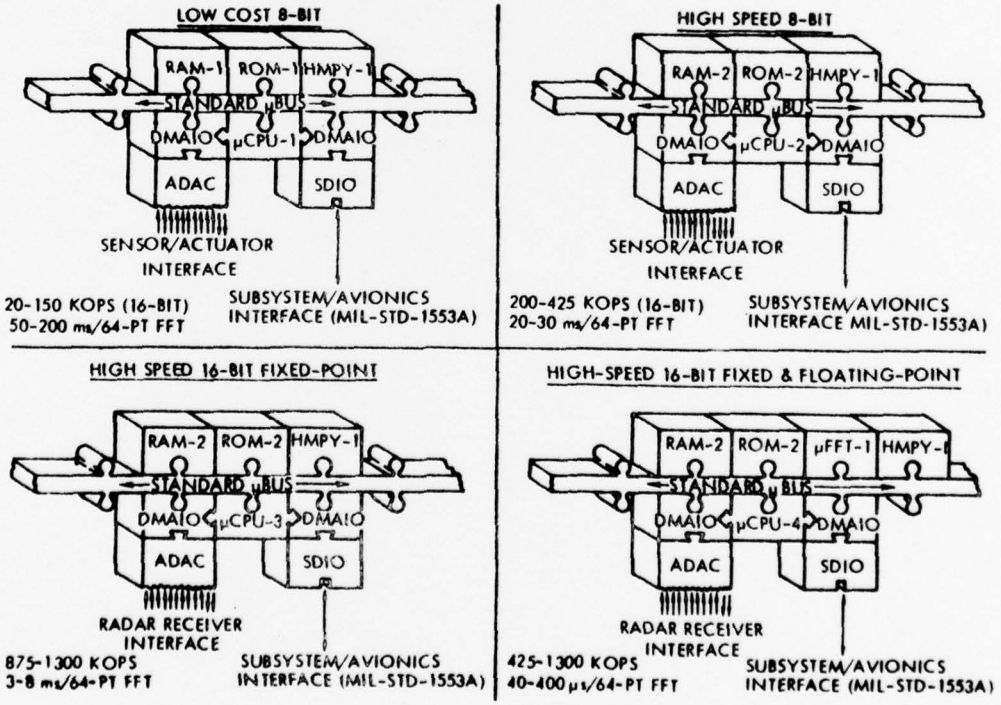


Figure 2 - Macromodular Microcomputer Family

integrated by a standard parallel microbus, (μBus) as a means of achieving configuration flexibility and multi-source procurement of each module. The bus itself was tailored to standard-industry, LSI semiconductor random-access and read-only memory (RAM) and ROM) interfaces, since, like Rome, all paths within a microcomputer lead to memory, and, being a simple interface, (data, address/chip-select, read/write), it had the additional merits of simplicity and reliability. Memory synchronization, i.e. the generation of data available status, not provided by memory chips, was assigned to each memory user module, in that, given the access and cycle time of the RAM or ROM, it could be treated as a conventional logical element with a known propagation delay.

The work performed during this phase of the contract was presented at the IEEE Computer Society Microprocessor Workshop at Johns Hopkins University, Laurel, Maryland, 27-28 June 1978, and will shortly be published as a feature article in the Society's "Computer" magazine.

1.2 Objectives and Scope

The objectives and scope of the Phase V study under the extension of Contract N00014-75-C-0549, as defined in the Statement of Work, are as follows:

1. Based upon the macromodule definitions and specifications developed in Phases III and IV, determine the functional configuration, performance and interfaces of a microbus interface module (MIM), for use as a common element in all microbus modules. Document and design requirements in the form of a separate product function specification.

2. In accordance with the MIM design requirements, design requirements, design a breadboard module to interface a standard-industry, 8-bit microprocessor to the microbus and compatible semiconductor memory modules. Generate logic and associate timing and wiring diagrams for implementation with standard-industry SSI/LSI circuits.

3. Fabricate and test a breadboard assembly of the MIM design using a standard-industry wirewrap circuit board and commerical dual-in-line-package (DIP) integrated circuits.

4. Design end code a test program to run on the microprocessor when interfaced with the MIM and compatible read-write memory modules. The program shall be designed to verify the integrity of the microprocessor/MIM/RAM combination.

5. Using the test program verify the proper transfer of data/instructions across the MIM. Tests shall be conducted under maximum microbus length and loading conditions as specified in the MIM design specification. MIM and microbus propagation delay times shall be measured together with microbus signal waveform rise and fall times at the inputs and outputs to the bus. These test results, together with the MIM logic design and timing data, shall be included in the final report.

The intention being to validate the MIM concept in terms of a working model using standard-industry semiconductor circuits.

2. SUMMARY & CONCLUSIONS

The rapidly developing microprocessor technology poses serious standardization problems for the user, particularly the military, where logistics support costs are significant over the life cycle of tactical systems. Whereas standard interface buses are now in existence e.g. (S-100, Intel Multibus, National Microbus, Motorola Microbus, European "MUBUS"), no two buses are the same.

To provide freedom of choice in microcomputer components throughout a system life cycle, a programmable microbus interface module (MIM) using common programmable control elements (PCEs), such as that described in this report, absorbs the interface irregularities of commercial microprocessors memory and I/O modules, thereby allowing the selection of components based on performance, support software, cost and other driving factors. Further, having made the choice of microprocessor for a given application, the user need not feel committed for all time should, for example, the requirements grow to exceed the capabilities of the processor or a more desirable μP appear on the market at a later date. The same rationale applies to I/O devices such as A-D and D-A convertors, MIL-STD-1553A/B serial interface units and others which are continually undergoing competititve improvement.

3. MICROBUS INTERFACE MODULE (MIM) DESIGN & APPLICATION

Since the definition of the standard μBus, (Fig. 3), some three years ago, individual microprocessor manufacturers have established their own unique bus structures inhibiting the option of swapping one microprocessor or I/O module for a more desirable alternative from a different manufacturer, at any time during the system life cycle. Such a module swapping feature has particular significance in the midst of today's rapid and random evolution of microprocessors and supporting interface devices. Further, whereas a certain degree of machine independence can be achieved in software through the use of a suitable high order programming language, no such "hedge" currently exists in the hardware world. Hence, in order to achieve independence in microcomputer product selection, a programmable microbus interface module (MIM) has been defined and fabricated, and is described in the following paragraphs. [6]

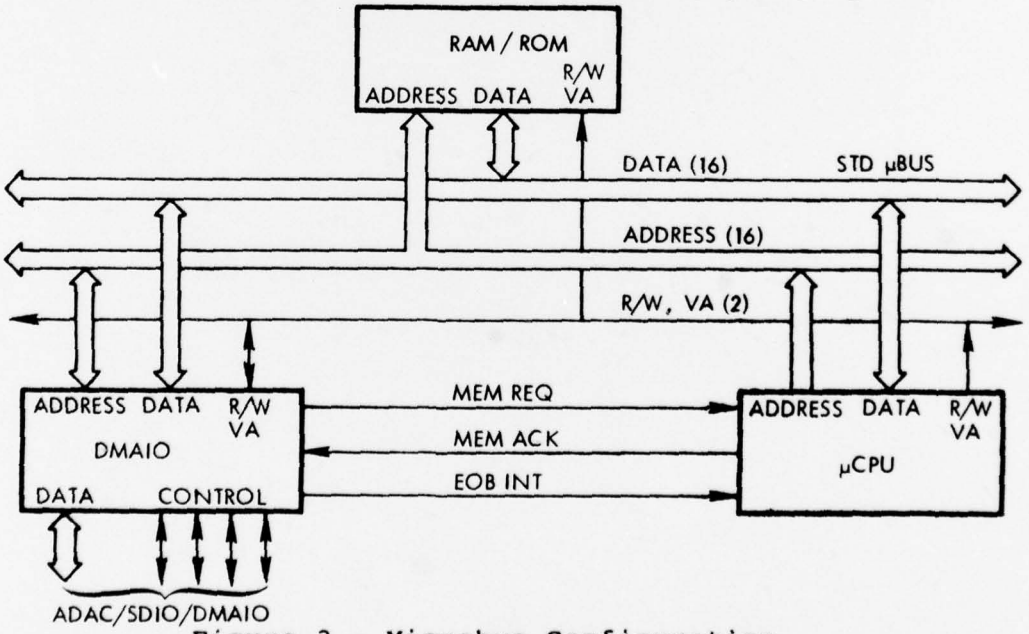


Figure 3 - Microbus Configuration

3.1 System Design Requirements

The MIM is basically required to provide a programmable interface between standard-industry microprocessors, input-output data conversion devices, RAMs, (E/P) ROMs and a common μBus, Figure 4. As such, the MIM, is in effect, a high-speed controller which continuously samples the status of irregular/non-standard control lines from a given device and translates these into a regular/standard form in synchronism with data and memory address information. In terms of speed and propagation delay the MIM must maintain the normal instruction execution times of the microprocessor.

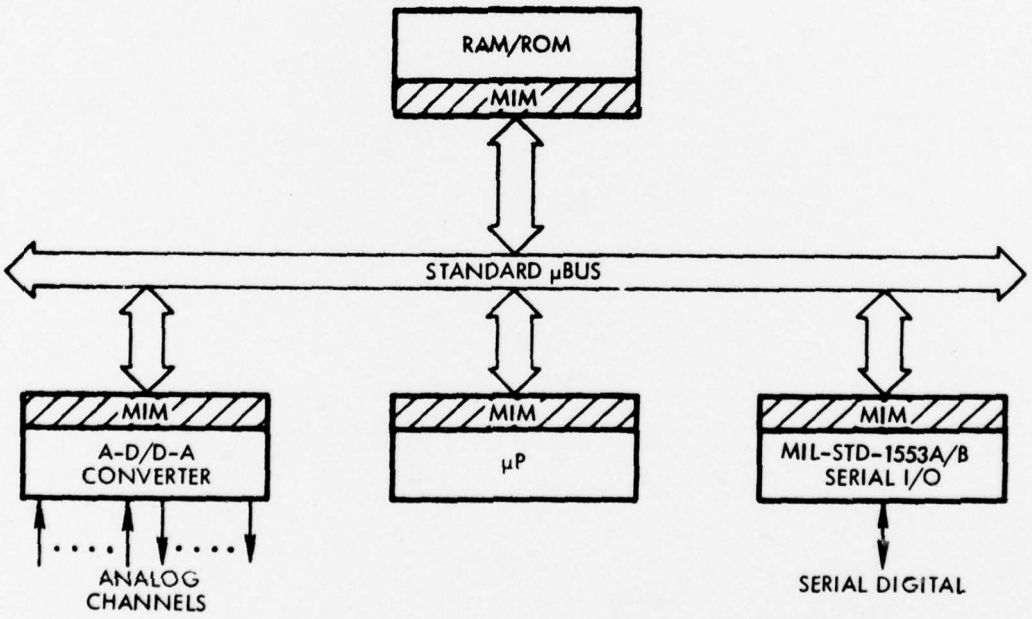


Figure 4 - Multi-Source Microcomputer Product Integration with Programmable MIM

3.2 Common Programmable Control Element (PCE)

Since the MIM is required to perform a similar function in each major microcomputer (μC) component a common programmable control element, (PCE), was defined for very large scale integration (VLSI). The basic functional relationship of this element to the μC component and microbus is shown in Figure 5. The control and status signals of any given μC component are sampled synchronously with the system clock by the control element, which translates these discrete information states into appropriate control signals to the bus and microcomputer component.

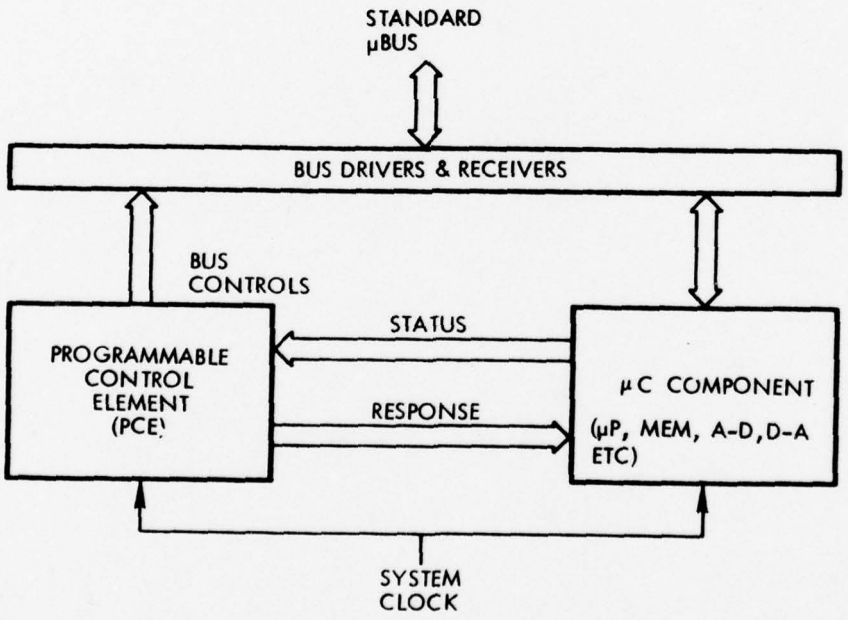


Figure 5 - Common Programmable Control Element

A compatible structure for such a control element is of the form shown in Figure 6, which is fundamentally a device capable of performing state transitions based upon the current state of the outputs and the logical status of one or more of the C component's status lines. An input register is used to store the latter inputs between clock pulses, with the controller section containing the necessary conditional branching logic to generate/access the next output state/microinstruction. In terms of interfacing with the I8080A, M6800 and various analog and digital I/O components, discussed in subsequent paragraphs, up to 16 input and 20 output lines were found adequate for each PCE. Additional I/O requirements could be met by distributing the control among several PCEs.

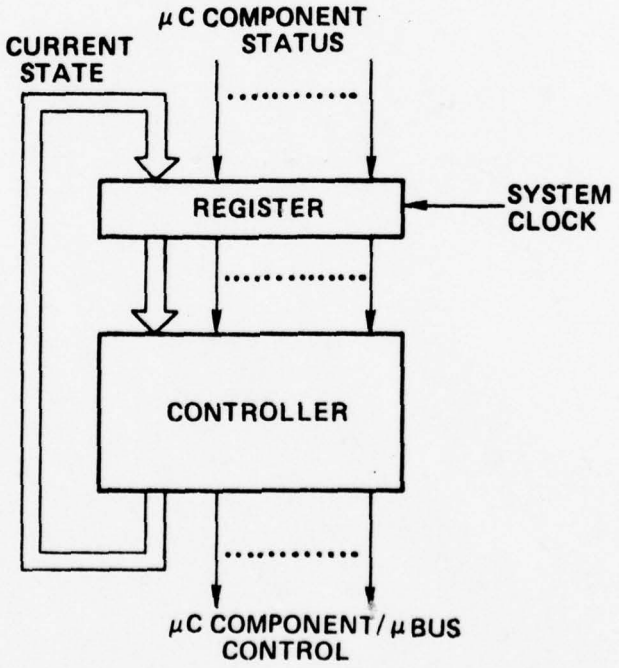


Figure 6 - Basic PCE Structure

3.3 Design Approaches

To achieve the design goals outlined above four candidate methods of implementing the controller section of the PCE were reviewed. For completeness, hardwired logic is included, although the lack of flexibility in this approach was the primary reason for exploring programmable alternatives. The salient characteristics of the four approaches can be summarized as follows:

- o Inflexible, hardwired standard-industry SSI/MSI logic circuit interconnections
- o New logic design and wiring per μC component

2. Standard Cell LSI Arrays

- o Mask/factory programmed cell/logic interconnects
- o New logic design and masks per μC component

3. Field Programmable Logic Arrays (FPLA)

- o Electrically/field-programmed Boolean equations
- o New program per μC components

4. Programmable Read-Only Memories (PROMs)

- o Electrically/field-programmed, microprogram
- o New program per μC component
- o Speed inversely proportional to capacity

The two most attractive means of implementing the controller section of the PCE lie in field programmable logic arrays (FPLAs) [7,8] and small programmable read-only memories (PROMs),

since both of these have speeds similar to hardwired logic circuits and, in addition, provide the field programming feature. Available FPLAs in 16x48x8 configurations exhibit typical propagation delays of 35 nsec and 32x8 PROMs, 25 nsecs. These delays are comparable to those of hardwired logic interface circuits such as the Intel 8228. Further, the FPLA possesses a "don't care" response feature without the speed penalty of a PROM with a large address decoded.

3.4 Selected Approach

In the light of the above performance requirements and available hardware alternatives, a combination of the FPLA and PROM design approaches was used for the breadboard model of the PCE, (Figure 7). The FPLA and PROM sections can either be used independently or linked together externally depending upon the application. As a whole unit the PCE functions as follows:

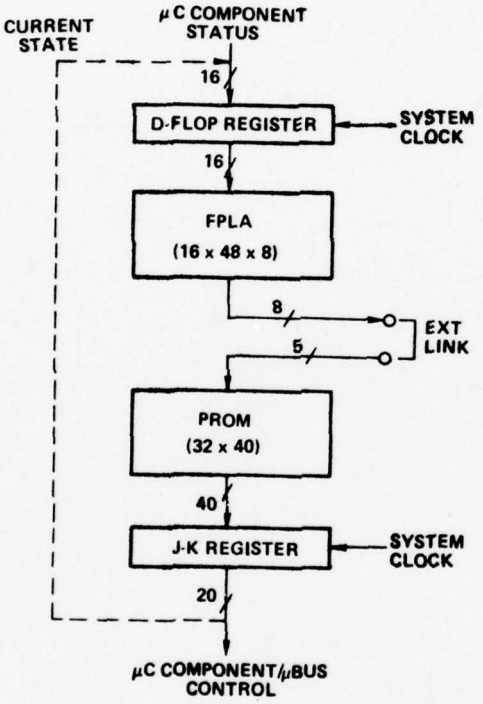


Figure 7 - Breadboard PCE Configuration

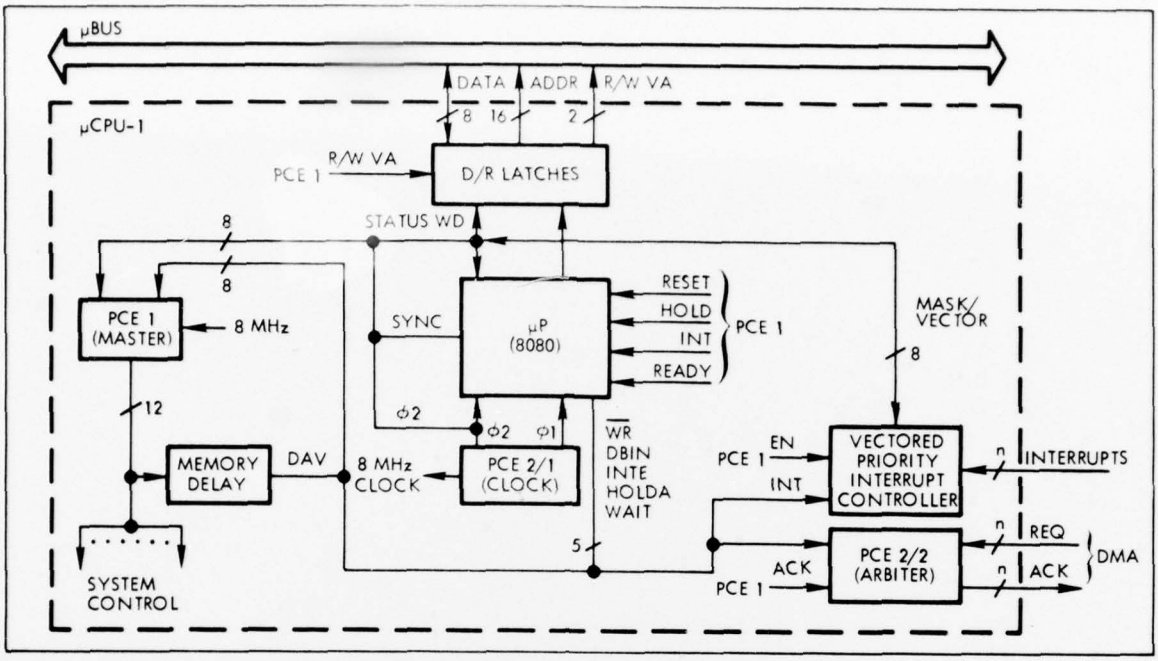
A 16-bit high-speed D-flop register samples and stores the current state and μC component status line information synchronously with the μC clock. One 16x48x8 FPLA performs both the conditional branching logic and PROM address generation functions. Input conditions requiring no change in output control state are programmed as "don't care" conditions in the FPLA, such that the first location in the PROM is always addressed. The latter contains thirty-two 40-bit microinstructions to provide both the true and complement states of a 20-bit word to the output J-K flip-flop register. The "don't care"/"do nothing" microinstruction, containing all zeroes, is ignored by the J-K register, thereby maintaining the previous output state. Using standard-industry Schottky bipolar SSI/MSI/LSI circuits, the accumulative propagation delays from input to output total 71 nsec (typical), 106 nsec (maximum), allowing 8 MHz minimum sampling/clocking. The latter rate meets the requirements of currently available standard product μC components, with the option of using higher speed device technology, if required, for the VLSI version of the PCE.

3.5 MIM Applications

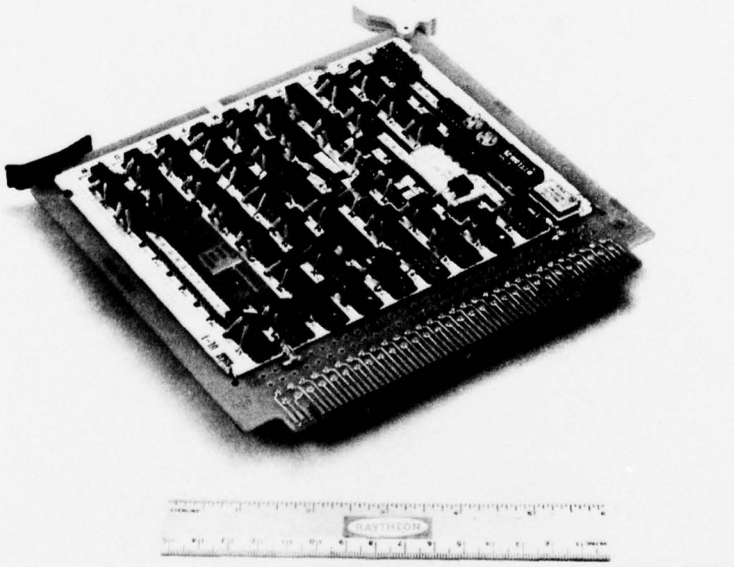
Using the PCE as a basic building block for the MIM, four microcomputer macromodule applications are described in the following paragraphs. One control element is required for memory mapping and interface, two for microprocessor interfacing, and up to four elements are required for certain I/O products.

3.5.1 Microprocessor MIM

Of all the individual microcomputer component interface requirements, microprocessors present the worst case for speed and complexity. Figure 8 shows an Intel 8080-based μCPU-1 macromodule



(A) Block Diagram



CN-6-6546

(B) Breadboard Model

Figure 8 - Microprocessor MIM

using two programmable control elements (PCEs) to absorb the irregularities of the 8080 versus other alternative μPs. PCE1 is termed the master PCE since it performs the main μP/μBus interface function. PCE 2 is used to generate the 8080-peculiar clock waveforms, and to control μBus/memory access for direct memory access (DMA) I/O channels.

Master PCE (PCE1) - Figure 9 shows the functional configuration of PCE1. An input multiplexer selects either one of two sets of 16 inputs from the data or control lines of the 8080 together with the current state information contained in the output register. Figure 10 shows the input/output word formats and individual bit assignments for PCE1 as they apply to the Intel 8080. The data output lines of the 8080 (D_{0-7}) together with "SYNC" and "ϕ_2" are normally routed by the multiplexer to the FPLA inputs to respond to the machine status when "SYNC" and "ϕ_2" are at logic '1'. Conversely, when the latter outputs are at logic '0', the FPLA "MUX SEL" field selects the miscellaneous control outputs of the 8080.

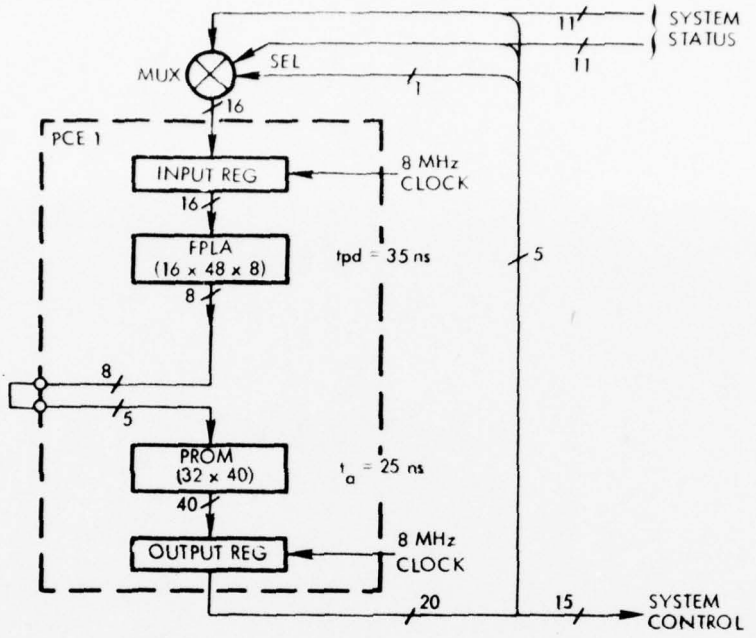


Figure 9 - Master Control Element (PCE1)

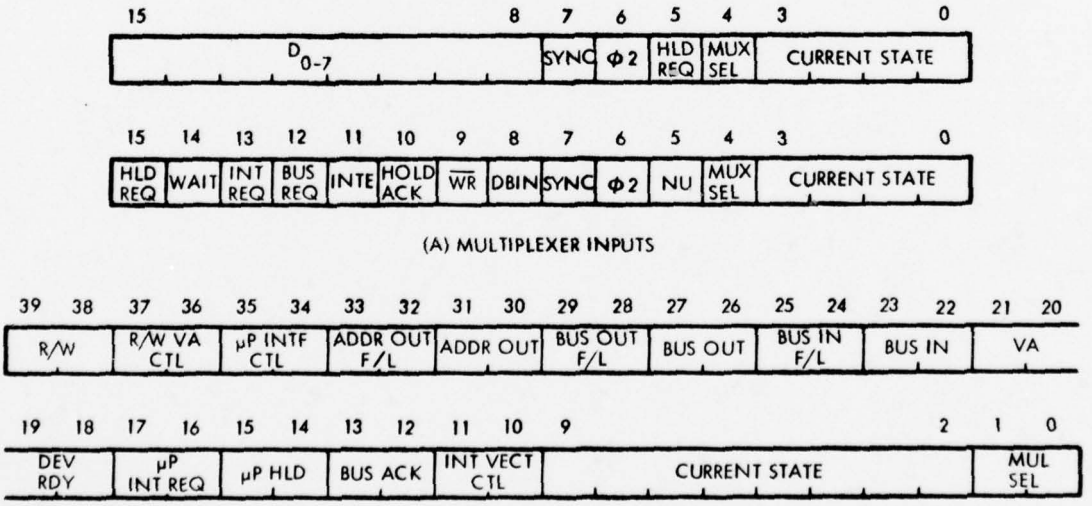


Figure 10 - Master PCE Input/Output Control Word Formats

Clock Waveform Generator (PCE2/1) - To synchronize the operation of the master PCE with the microprocessor and provide the flexibility of generating various clock waveforms to suit any given microprocessor, one-half, (the lower-half), of a second PCE is programmed as a clock waveform generator, (Figure 8). A 20 MHz crystal oscillator is used to clock the output register, which in turn furnishes the current address to the PROM.

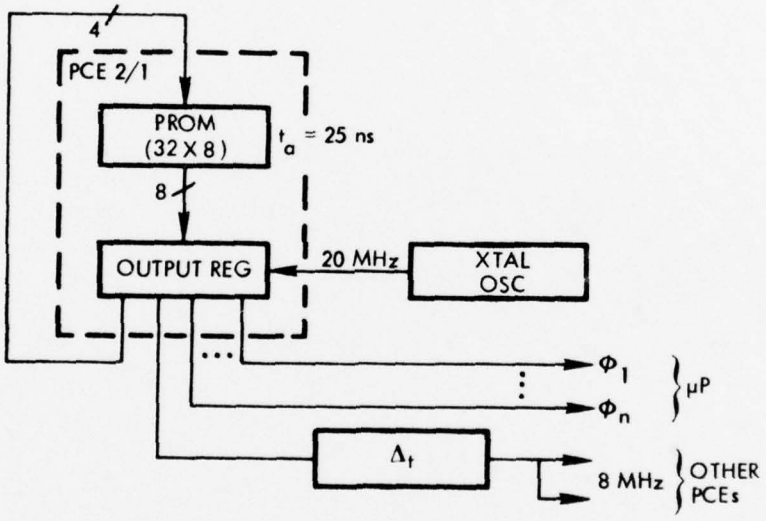


Figure 11 - Clock Waveform Generator (PCE2/1)

The PROM is programmed to provide any desired sequence of byte bit patterns such that, the individual binary bit sequences from byte to byte form a specific clock waveform and phase relationship with the other bit trains. A delay line (Δt) adjusts the phase of the 8 MHz clock outputs to PCE 1 in relation to the microprocessor clock phases, to synchronize PCE 1 sampling with the μP output waveforms.

Swapping Microprocessor Types - To illustrate the adaptability of the MIM Hardware to accommodate alternative microprocessor types, the Intel 8080 was replaced by the Motorola 6800, (Figure 12). PCE1 and PCE2 required the reprogramming of FPLAs/PROMs to interpret the 6800's outputs and generate the 6800-peculiar clock waveforms.

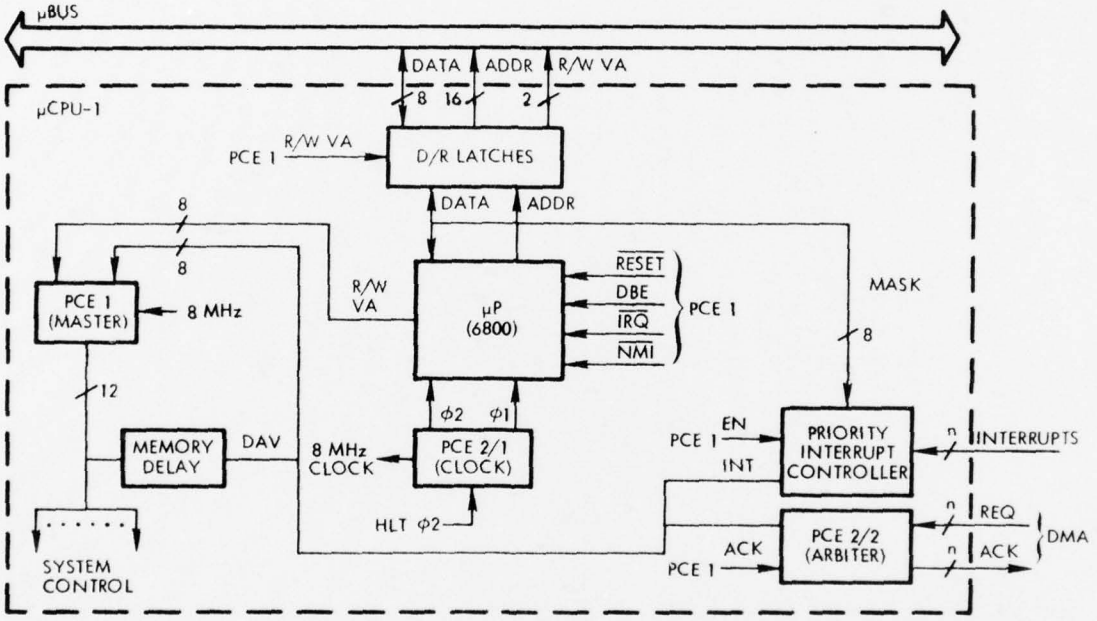


Figure 12 - μCPU-1 With M-6800 in Place of Intel 8080

3.5.2 Memory MIM

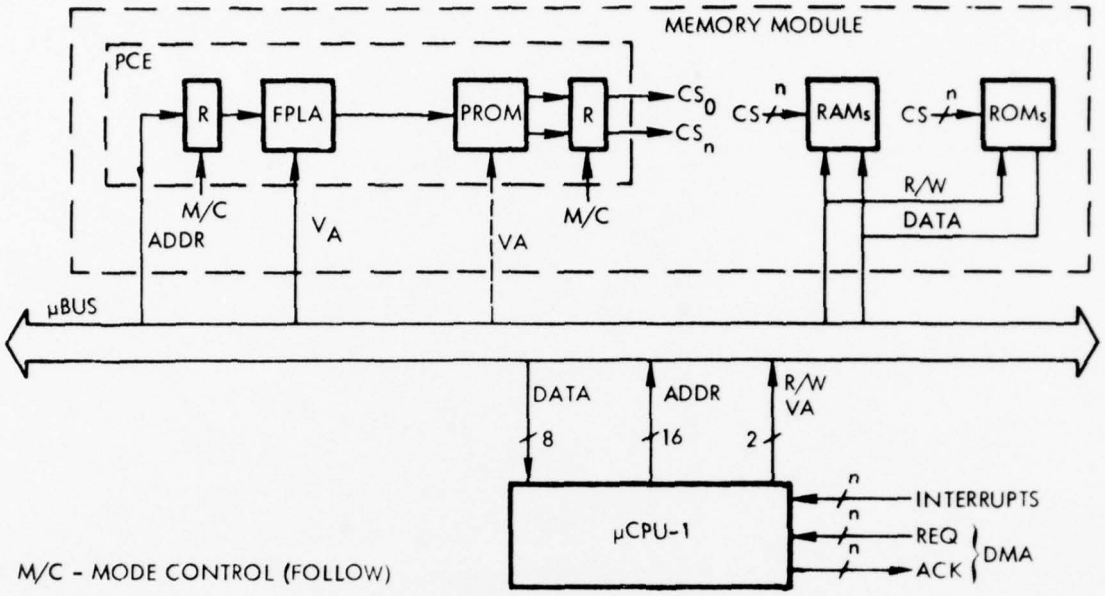
At the present time LSI semiconductor RAMs and (P)ROMs vary in their electrical interfaces according to the manufacturer. Ideally, semiconductor (S/C) memory chips should be word or byte organized with binary-coded chip select the word select inputs for direct interface to the memory address lines of the μBus (in the same way I/O modules are interfaced). Nevertheless, since variations in RAM and (P)ROM interfaces can be expected to continue for several years, the programmable PCE approach offers two features:

1. Choice of any manufacturer's RAMs and (P)ROMs without interface redesign.

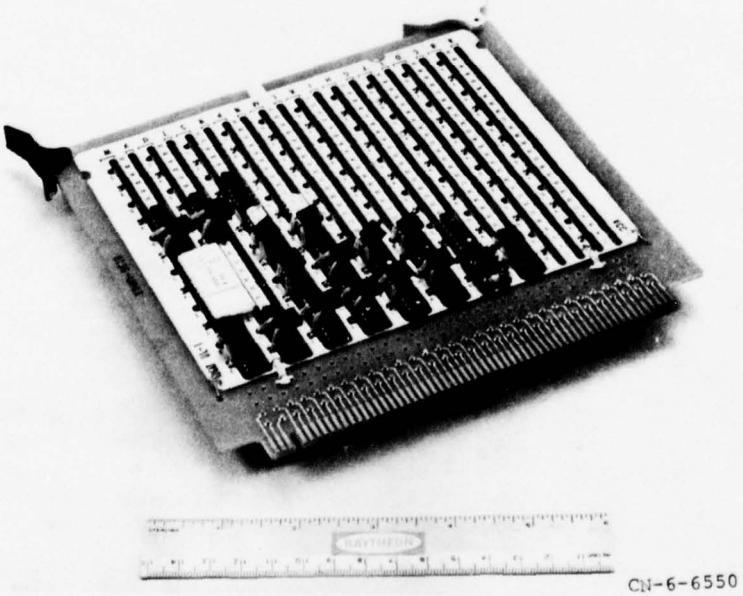
2. Mapping of data and program memory locations on a module basis to suit any given application.

Figure 13 shows the use of a PCE to generate S/C memory chip select signals for the main memory of the microcomputer. The µBUS address lines are translated by the FPLA into PROM addresses, (simultaneously with the MIM operation), which, in turn, access unary-coded chip select words, each covering a range of memory locations and corresponding RAM or ROM memory chip. While small memories consisting of up to eight chips could be accommodated by the FPLA alone, larger memories require the longer word length, (and number of bits/chip select lines), more easily obtainable from PROMs.

3.5.3 DMA Control (PEC2/2) - External requests for access to the µBus and memory are handled by the upper half of PCE 2 (Figure 14). Up to seven request lines can be sensed and, given µBus availability from the microprocessor, one of the seven requests is honored according to the priority pre-programmed in the FLPA.



(A) Block Diagram



(B) Breadboard Model

Figure 13 - Memory MIM

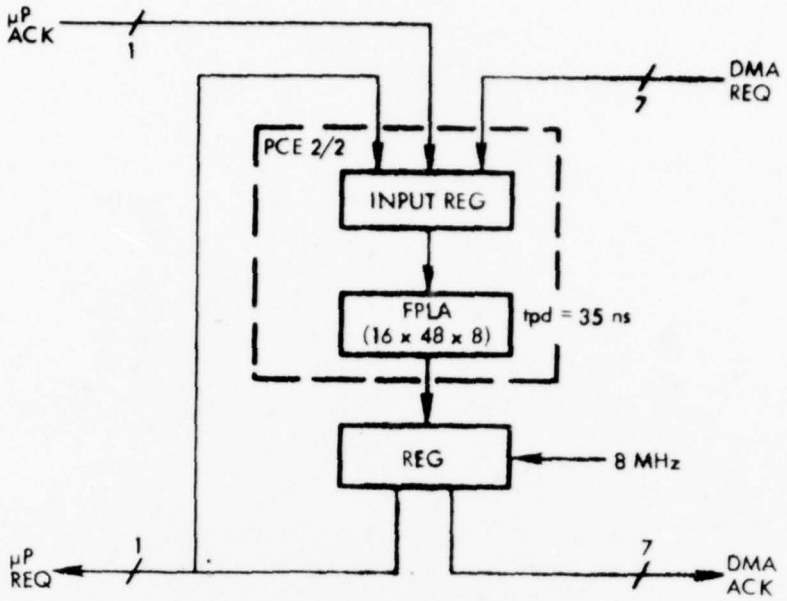


Figure 14 - DMA Control (PCE2/2)

3.5.4 I/O Module MIMs

Recent large scale integration (LSI) activity in data acquisition and conversion products has made available virtually whole devices in a single LSI package with similar irregular interfaces to microprocessors. Three such standard-product I/O modules have been interfaced to the μBus using the MIM approach. All modules contain small buffer memories, mapped as part of the main memory, such that data is loaded/accessed at these storage locations either by the microprocessor under program control or by the data acquisition/conversion device.

A-D and D-A Convertor MIM - The analog to digital, digital to analog convertor (ADAC) macromodule of Figure 2 has been configured using standard product LSI A-D and D-A convertor modules and three PCEs as integration element (Figure 15). Two separate PCEs, (PCE 1 and 2), are assigned to each buffer memory for μBus address decoding and data transfer control. PCE1 controls access to the A-D buffer memory, (an 8-word x 12-bit, 2-port RAM), and PCE 2 similarly controls an 8-word x 8-bit discrete register file for the D-A convertors. PCE3 controls the selection, conversion and transfer of quantized analog data into the 2-port RAM.

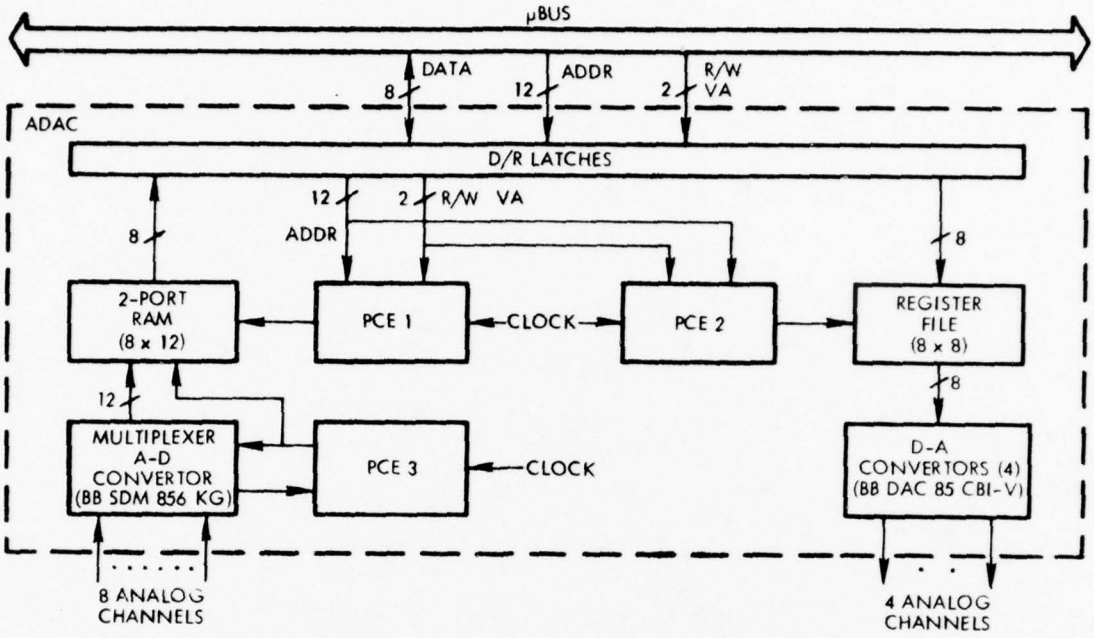


Figure 15 - ADAC Macromodule Using Standard Product A-D and D-A Convertors and Three PCEs.

Serial Digital I/O MIM - Since the federated microcomputer system shown in Figure 1 interfaces with the avionics weapon control system (AWCS) via an umbilical connection before the missile is launched, a MIL-STD-1553A/B-compatible serial digital I/O is used. Several manufacturers supply the 1553A/B interface modules in varying degrees of completeness, but no standard parallel digital interface exists. Figure 16 shows a virtually complete 1553A/B-compatible, standard-product (SCI-MTI 100) serial I/O module interfaced and controlled by four PCEs. As in the case of the ADAC macromodule, separate PCEs (PCE1 and 2), are assigned to the local buffer memories for μBus access control, and two additional PCEs, (PCE3 and 4), sample the transmit and receive status and control lines of the serial I/O module with an appropriate programmed response to move the parallel message data word to/from the 2-port RAMs.

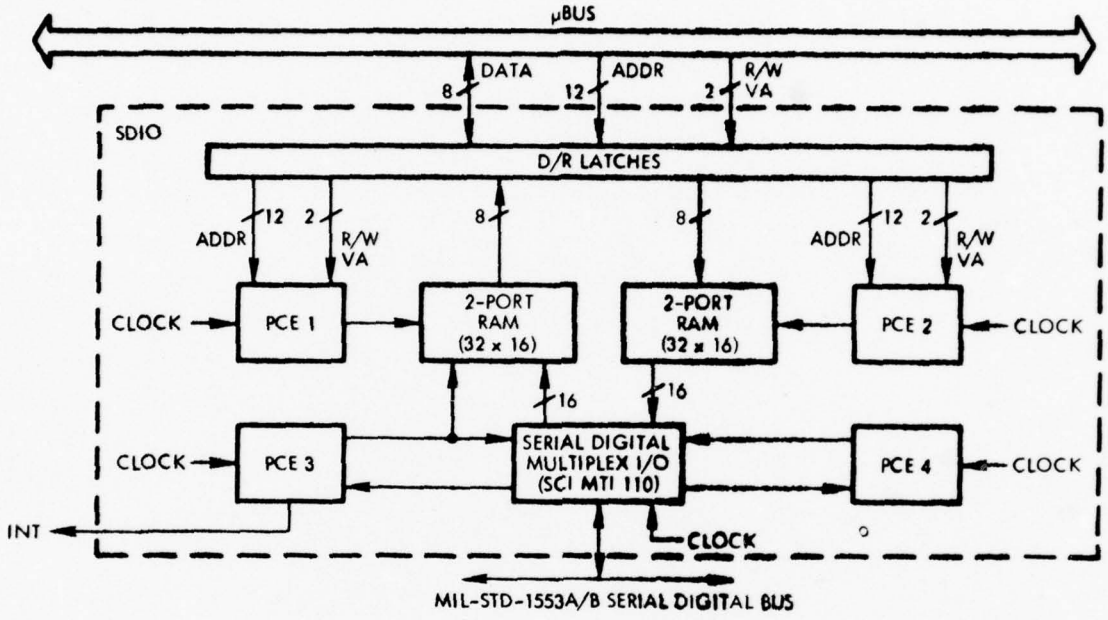


Figure 16 - SDIO Macromodule Using Standard Product MIL-STD-1553A/B Parallel/Serial Digital Convertor and Four PCEs.

4. MIM TEST RESULTS

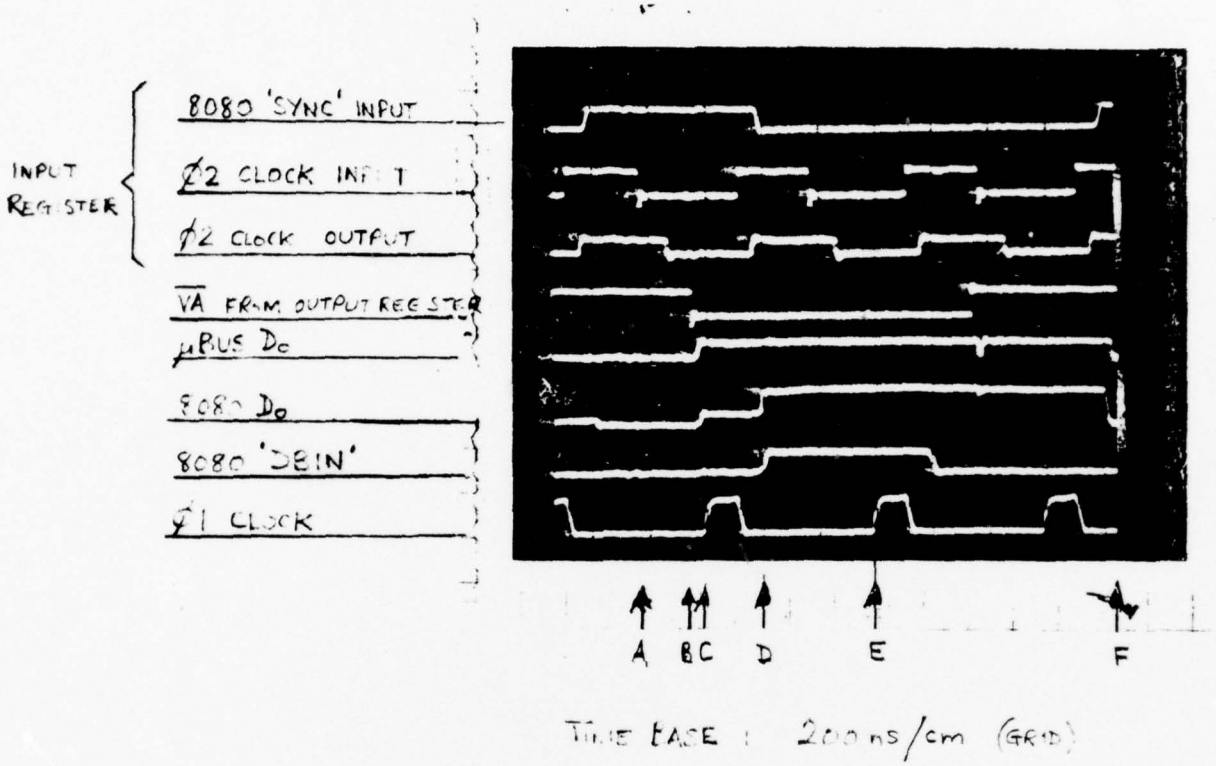
To validate the performance of the MIM, the response of each individual PCE to its respective set of input status was verified and the propagation delay from input to output measured. Signal waveforms were recorded to verify the quality of the pulse trains.

Following the checkout of each PCE the microprocessor and memory circuits were integrated as two separate macromodules, (μCPU-1 and RAM/PROM), via the standard μBus.

A test program was stored in the PROM and executed by the microprocessor. This program was written to exercise the load and store instructions of the μP repertoire, in order to move data to and from memory across the μBus and MIM interfaces. Instruction execution times were measured to verify that the MIM had no effect on the normal performance of the microcomputer.

4.1 PCE Performance

The FPLA and PROM programs were verified for each set of input conditions, and the propagation delay measured through the waveforms given in Figures 17 through 19.



Timing Marks

A. Address valid to begin a memory cycle (from 8080)
B. Input to FPLA to begin memory cycle
C. Data from memory ready
D. 8080 places data bus to input mode
E. 8080 strobes data in
F. Begin next cycle

Figure 17 - Master PCE Input/Output Waveforms

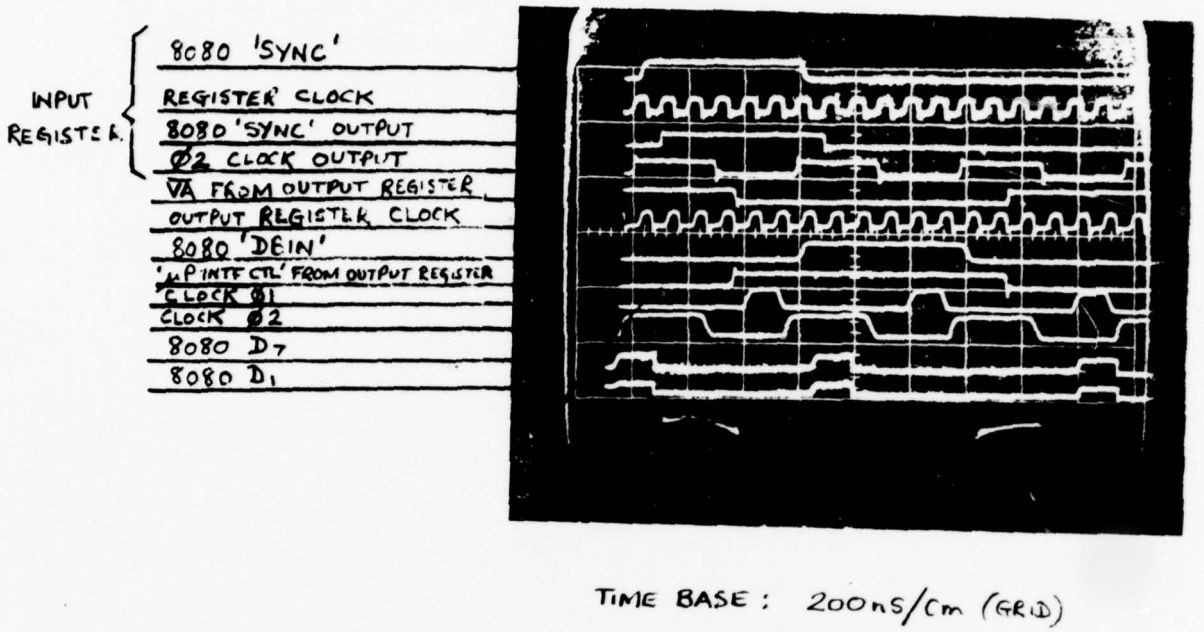


Figure 18 - Master PCE (PCE1) Input/Output Waveforms

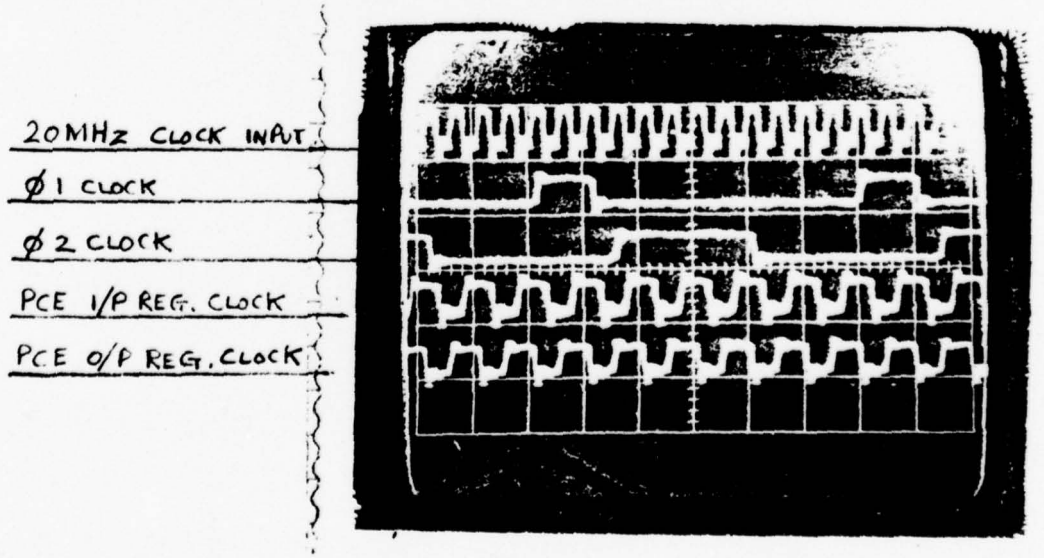
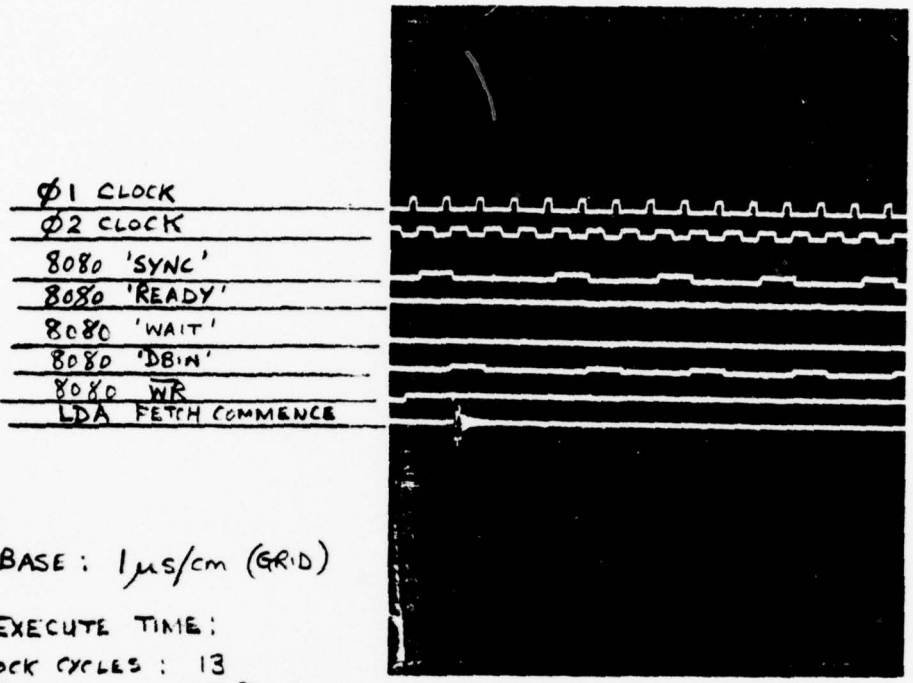


Figure 19 - Clock Waveform Generator (PCE2/1)
Input/Output Waveforms

From the above waveforms it can be seen that the Master PCE is capable of operating well within the 10 MHz sampling rate.

4.2 Microcomputer Performance

To determine the effect of the MIM on the overall performance of the microcomputer, the load and store instruction execution times were measured from the waveforms shown in Figures 20 and 21.



TIME BASE : 1 μs/cm (GRID)

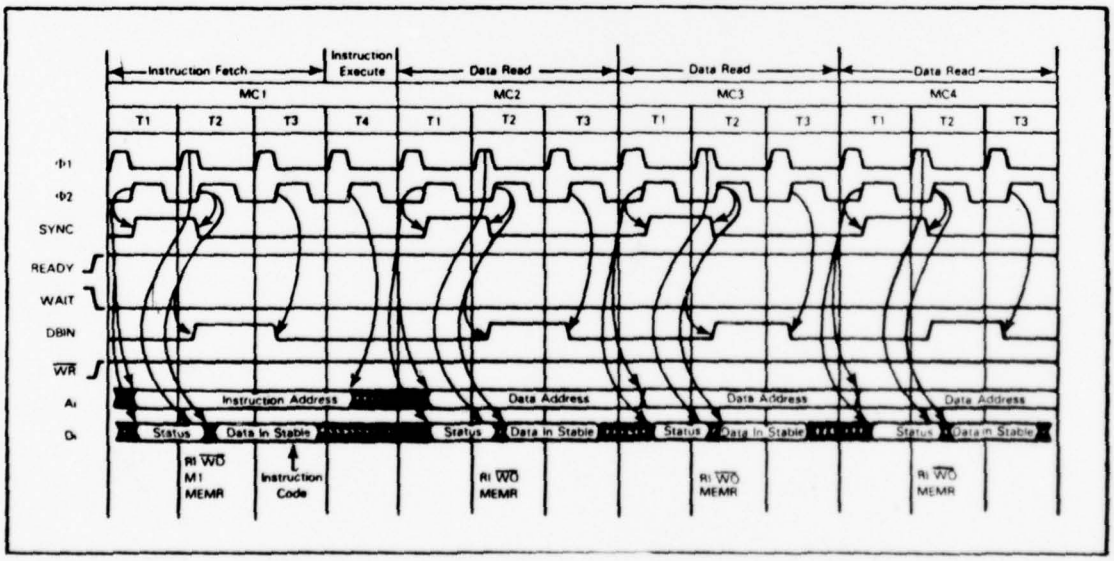
LDA EXECUTE TIME:

CLOCK CYCLES : 13

DURATION : 7.8 μs

(600ns / CLOCK CYCLE)

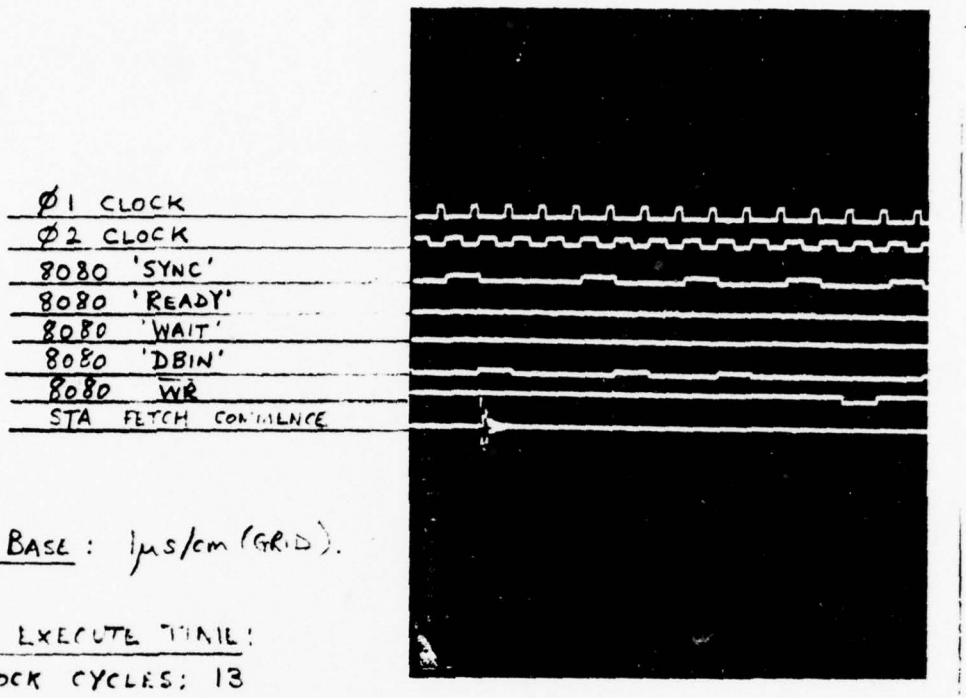
(A) MEASURED WAVEFORMS



SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: LDA

(B) MODIFIED WAVEFORMS (REF. 9)

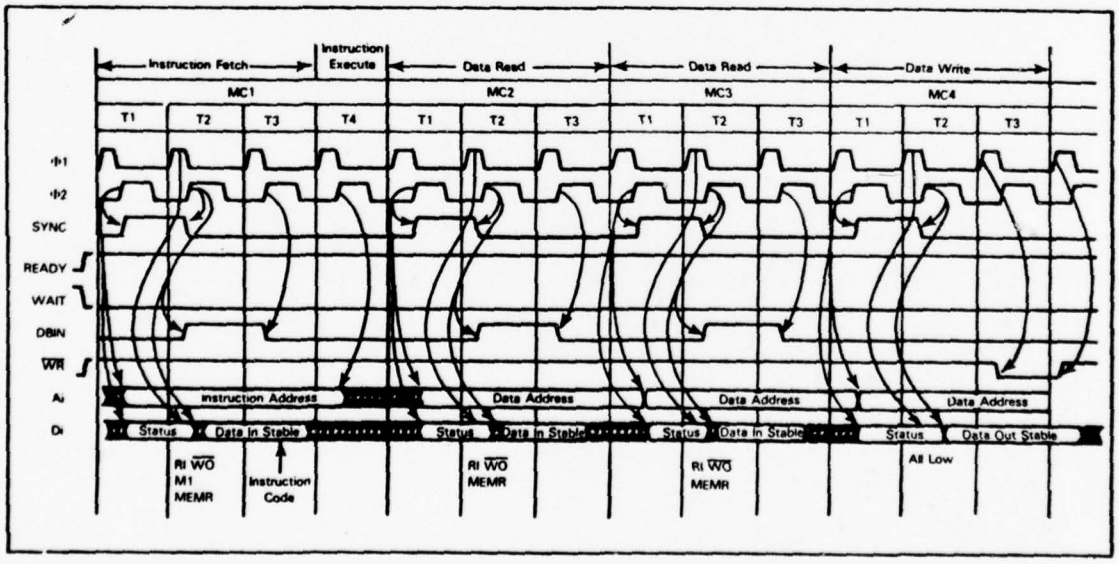
Figure 20 - 8080 LDA Instruction Fetch/Execute Waveforms



TIME BASE: 1μs/cm (GRID).

STA EXECUTE TIME:
CLOCK CYCLES: 13
DURATION: 7.8 μs
(600 ns/CLOCK CYCLE)

(A) MEASURED WAVEFORMS



SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
STA

(B) TIMING WAVEFORMS (REF. 9)

Figure 21 - 8080 STA Instruction Fetch/Execute Waveforms

The above waveforms indicate that the normal instruction execution times are being maintained with the MIM as an interface between the microcomputer components.

5. MIM STANDARD ELECTRONIC MODULE (SEM) PACKAGING

The MIM provides a flexible means of integrating a wide variety of standard-industry microcomputer components with a common μBus interface. As such, it constitutes a useful standard device for incorporation within the Navy's Standard Electronic Modules (SEMs). Hence, although not specifically called for in the Statement of Work, a preliminary investigation into SEM/PCE and SEM/MIM compatibility was made.

Through the use of hybrid LSI or leadless-carrier packaging techniques it is conceivable to package the PCE portion of the MIM on a 40-pin SEM 1A plug-in module, and the whole MIM on a 100-pin SEM-2A module.

5.1 SEM-1A PCE

The total chip count of a PCE, using standard-industry SSI/MSI/LSI circiuts, is 24. A 2" x 1" hybrid LSI package of the form described in the Phase III Study Report provides a practical intermediate VLSI package as a forerunner to a single monolithic chip PCE. Figure 22 illustrates a feasible SEM-1A PCE.

5.2 SEM-2A MIM

Using the 100-pin SEM-2A configuration, the entire interface between microcomputer component and the microbus, i.e. the MIM, could conceivably be mounted on one double-sided, plug-in module, using hybrid-LSI packaging of the PCEs and other supporting circuits, (Figure 23).

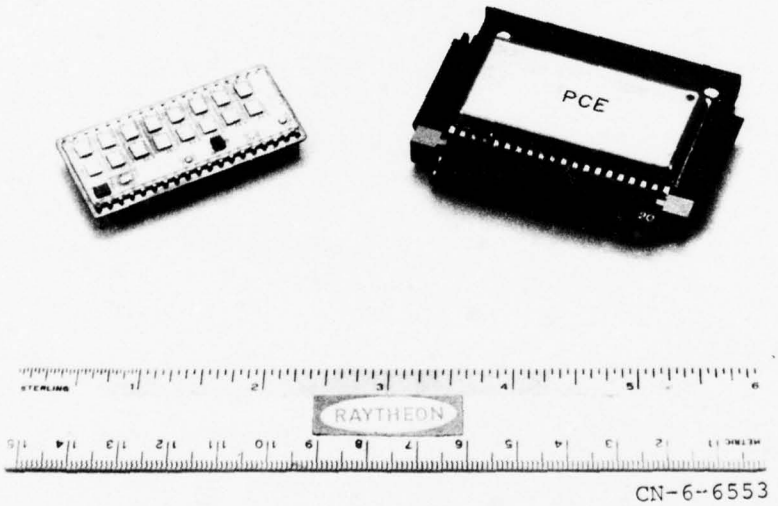


Figure 22 - SEM-1A Programmable Control Element

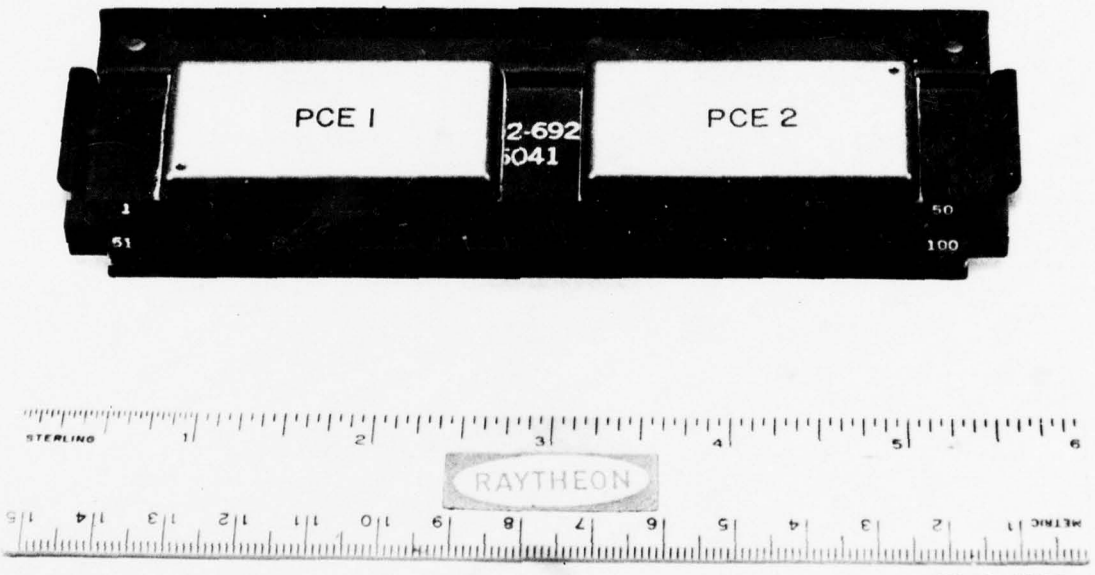


Figure 23 - SEM-2A Microbus Interface Module

However, due to the differences between MIM configurations for microprocessors, memories and I/O interface circuits, (see Figures 8 through 16), a series of three types of SEM/MIM would be required to accommodate the variations.

6. MIM LOGIC DIAGRAMS

The following pages of this report contain the detailed logic diagrams of the MIM as implemented in standard-industry SSI/MSI/LSI logic circuits, Figures 24 and 25. A circuit count by function is as follows:

6.1 µCPU-1 MIM

6.1.1 Master PCE (PCE1)

	Qty
Input Register	8
FPLA	1
PROM	5
Output Register	10
Sub. Total:	24

6.1.2 Clock Waveform Generator (PCE2/1)

PROM	1
Output Register	1
Sub. Total:	2

6.1.3 µBus Drivers/Receivers

5

µCPU-1 MIM Total: 31

6.2 µCPU-1 µP and Support Circuits

	Qty
Microprocessor	1
Master PCE Input Multiplexer	3
Clock Oscillator	1
Clock Delay Line	1
Clock Invertor	1
Clock Drivers	7
T^2L to MOS Convertors	3
Synch Flip Flops	1
Voltage Pull-Ups	1
Interrupt Control	2
Power On/Reset Driver/Logic	6
µCPU-1 Support Ccts:	27

6.3 RAM-2/PROM-2 MIM

FPLA	1
µBus Drivers/Receivers	5
RAM-2 MIM Total:	6

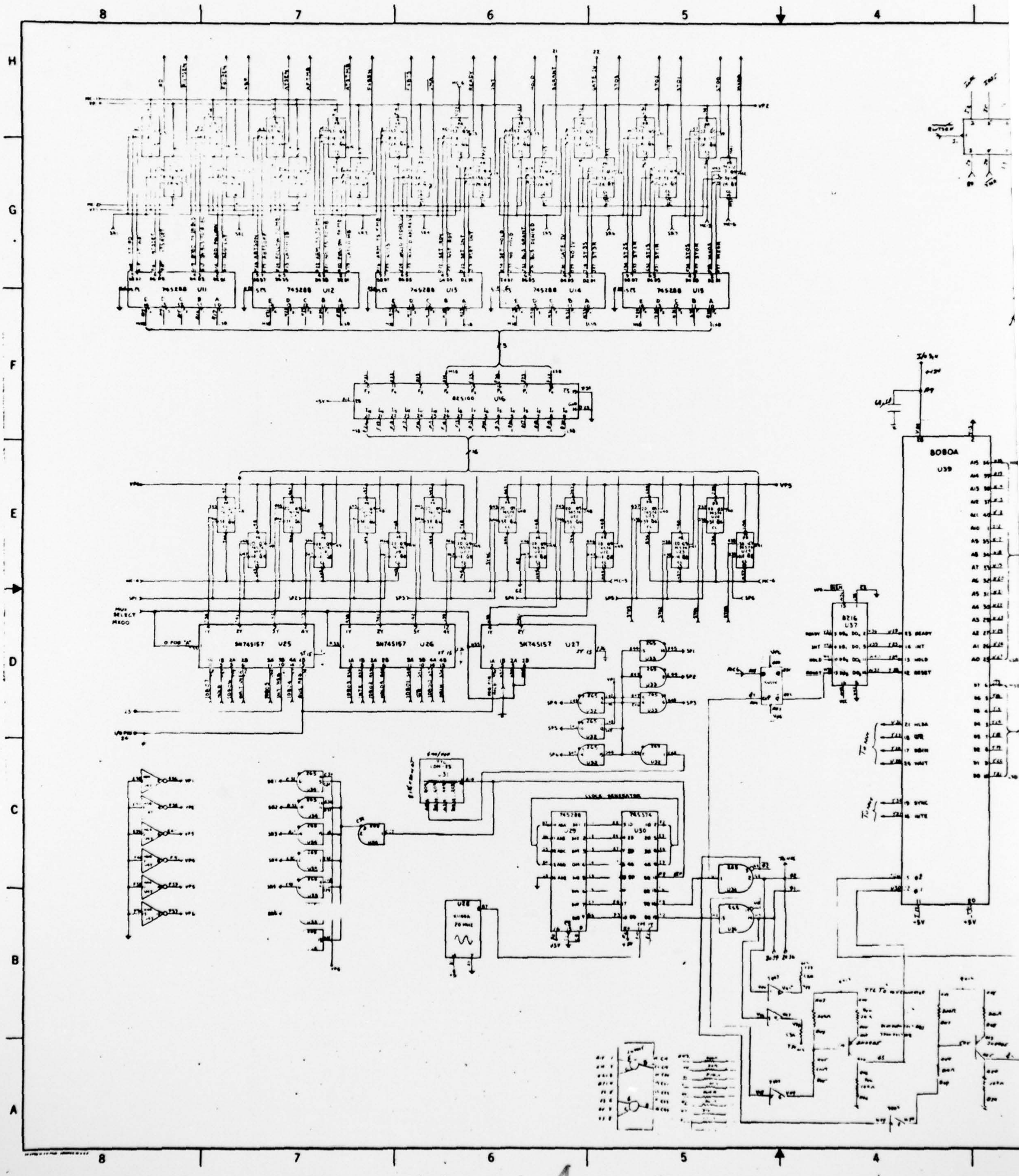
6.4 RAM-2/PROM-2 Memory Circuits

RAM	2
PROM	2
RAM-2/PROM-2 Ccts:	4

The major above functional areas are outlined on the following logic diagrams.

It can be seen that the circuit count of the μCPU-1 MIM could be reduced from 31 to 7 packages, using a monolithic LSI PCE instead of the 2-bit SSI input and output registers and separate FPLA and PROM circuits.

The remainder of the μCPU-1 circuits are required regardless of whether a hardwired or programmable MIM μBus interface is used.


8
7
6
5
4
H
G
F
E
D
C
B
A
74S288 U11
74S288 U12
74S288 U13
74S288 U14
74S288 U15
82S100 U16
SN74S157 U25
SN74S157 U26
SN74S157 U27
8216 U37
8080A
U39
CLOCK GENERATOR
74S288
U29
74S374
U30
U28
20 MHZ
READY
INT
HOLD
RESET
SYNC
WAIT
+5V

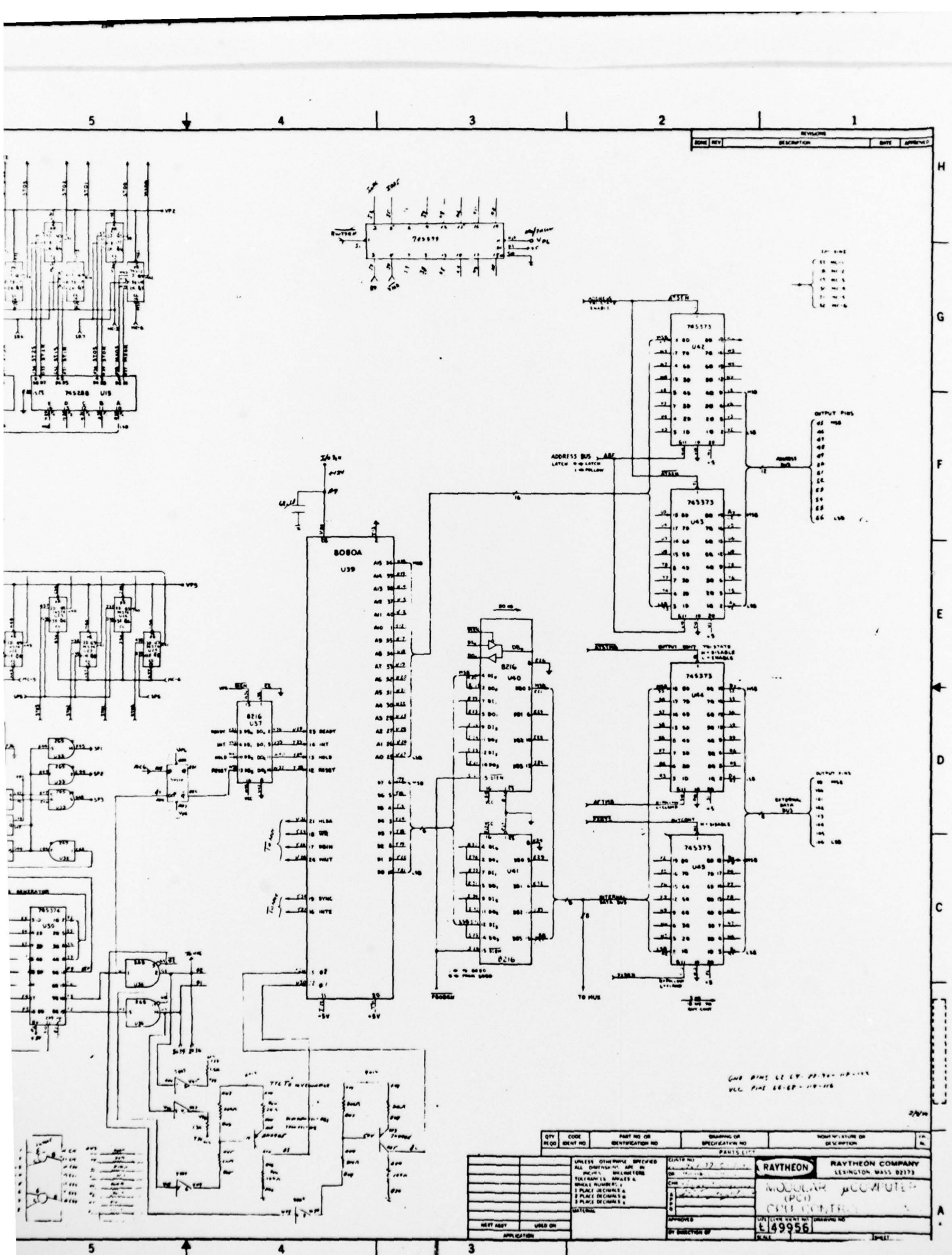
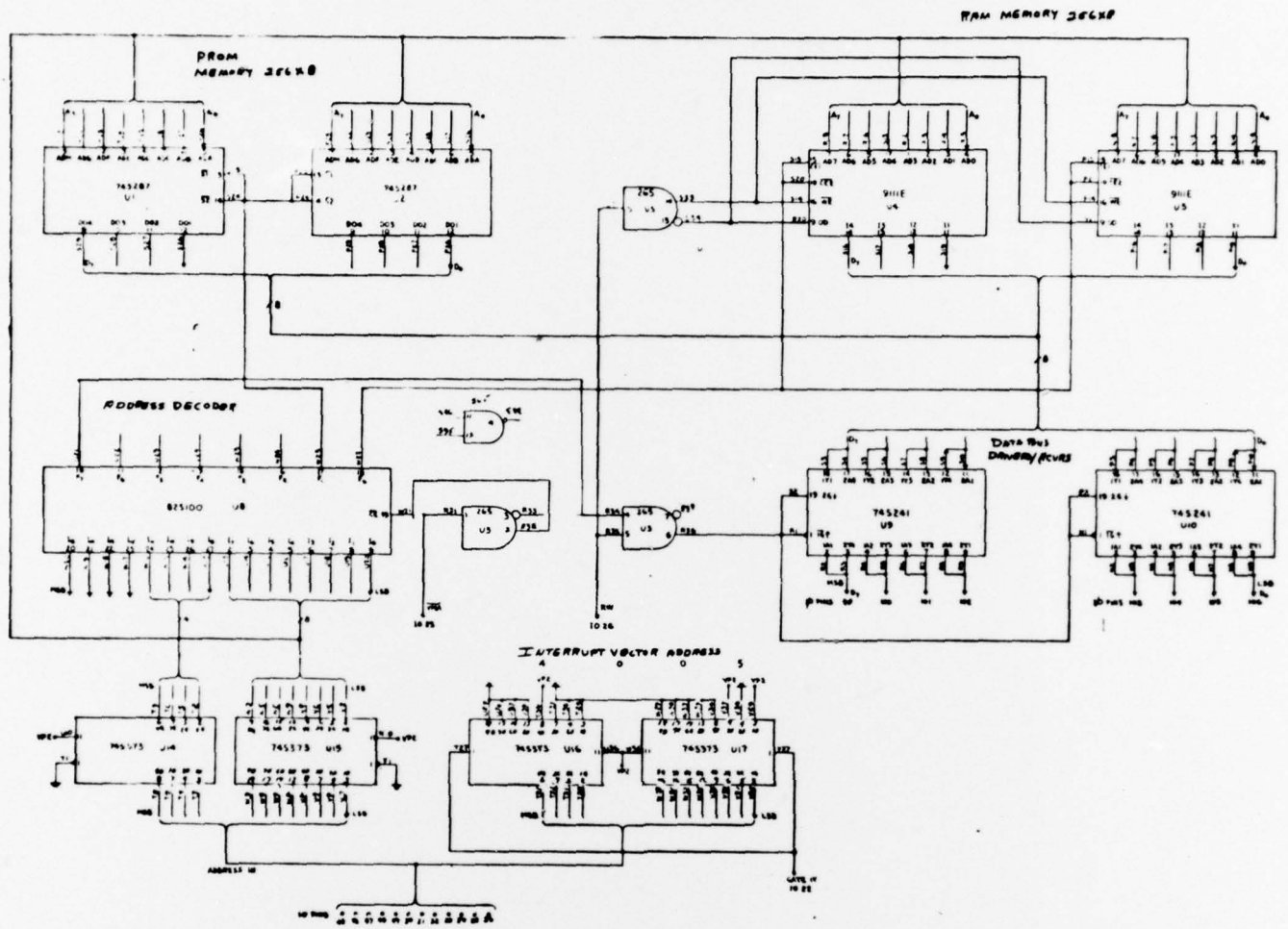


Figure 24 2 Page 42


RAM MEMORY 256X8
PROM
MEMORY 256X8
ADDRESS DECODER
Data Bus
Drivers/Recvrs
INTERRUPT VECTOR ADDRESS
A 0 0 5

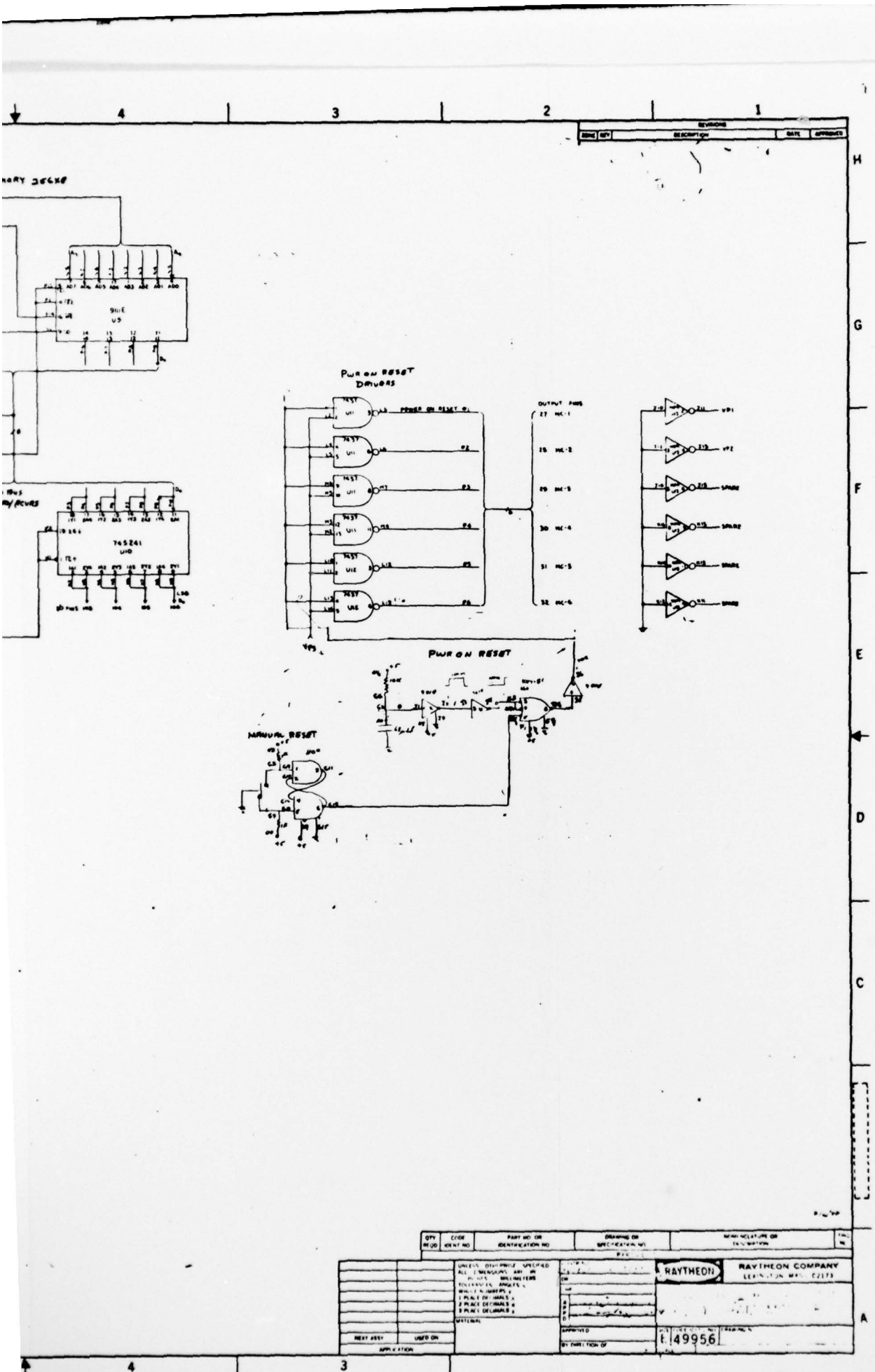


Figure 25

References:

1. Hall, B. A., and Trainor, W. V., "Modular Digital Missile Guidance System Study", Ph. I Report, 30 June 1974, DDC-AD-784-969/8GA.

2. Langley, F. J., Cooney, J. J., "Synchronous Microcomputer System for On-Board Missile Guidance and Control," 1975 National Computer Conference, Anaheim, CA., 19-22 May 1975.

3. Hall, B. A., and Langley, F. J., "Modular Digital Missile Guidance", Ph. II Report, 28 January 1976, DDC-AD-B010399L.

4. Langley, F. J., "Macro-Modular Microcomputer Family for On-Board Missile Guidance and Control," IEEE/NADC Microprocessor Standard Concepts Workshop, NADC Warminster, 22-24 June 1976.

5. Hall, B. A., Langley, F. J., and Wefald, K. O., "Computer Design Requirements for Digital Air-to-Air Missiles", AIAA Guidance and Control Conf., San Diego, CA., 16-18 Aug. 1976.

6. Langley, F. J., Demetrick, J., "An Adaptive Microprocessor/Microbus Interface Module", IEEE/NADC Annual Microprocessor Workshop, Johns Hopkins University, Laurel, MD., June 27-28, 1978.

7. Miles, G., "FPLAs Offer a Design Alternative for Development of System Logic," EDN Magazine, 5 Nov. 1975.

8. Cavlan, N. and Cline, R., "FPLA Applications - Exploring Design Problems and Solutions," EDN Magazine, 5 April 1976.

References (continued):

9. "The 8080A/9080A MOS Microprocessor Handbook" Advanced Micro Devices, 1977.

DISTRIBUTION LIST

Air Force Avionics Laboratory
Wright Patterson AFB, Ohio 45433
- AFAL/DHE (MAJ J. A. Decaire) (1)
- AFAL/DHM (Mr. R. E. Conklin) (1)

Air Force Systems Command
Andrews AFB, Md 20334
- AFSC/DLCA (Mr. P. Sandler) (1)
- AFSC/SDZ (COL R. Loukota) (1)
- AFSC/XRL (COL F. Smith) (1)

The Analytical Sciences Corporation
6 Jacob Way
Reading, Mass 01857
- Mr. C. F. Price (1)

Armament Development and Test Center
Eglin AFB, Florida 32542
- ADTC/DL (COL A. D. Brown) (1)
- ADTC/SD7 (Mr. G. Kirby) (1)
- ADTC/ADDE (Dr. J. W. Jones) (1)
- ADTC/DLMI (LCOL Britton) (1)
- ADTC/DLMT (MAJ E. Halprin) (1)

Chief of Naval Operations
The Pentagon
Washington, D. C. 20350
- NOP-982El (CDR K. H. Cox) (1)
- NOP-987P3 (Mr. W. B. McCall) (1)

DCASR
Raytheon Company
Wayside Ave.
Burlington, Mass 01803 (1)

Defense Documentation Center
Bldg. 5, Cameron Station
Alexandria, VA 22314 (1)

Director of Defense Research and
Engineering
The Pentagon
Washington, D. C. 20350
Mr. M. Keller (Rm. 3E1081) (1)
LTC G. Kopcsak (Rm. 3D1089) (1)

Harry Diamond Laboratory
2800 Powder Mill Road
Aldephi, MD 20783
Dr. Carter (1)

Institute for Defense Analysis
400 Army Navy Drive
Washington, D. C. 22202
Dr. T. C. Bartee (1)
Mr. G. W. Preston (1)

National Aeronautic and Space
Administration
Headquarters
Washington, D. C. 20546
NASA-KC (Mr. W. E. McInnis) (1)

National Aeronautic and Space
Administration
Jet Propulsion Laboratory
4800 Oak Grove Dr.
Pasadena, CA 91103

NASAJPL-114-122 (Mr. P. E. Lecoq) (1)
NASAJPL-114-122 (Mr. M. Ebersole) (1)
NASAJPL-158-205 (Mr. R. E. Covey) (1)
NASAJPL-/T1180 (Mr. R. W. Scott) (1)

Naval Air Development Center
Warminster, PA 18974

NADC-2031 (Mr. C. M. Nowicki) (1)

Naval Air Systems Command
Washington, D. C. 20361

NAIR-03P2 (Mr. J. W. Malloy) (1)
NAIR-03P3 (Mr. R. H. Krida) (1)
NAIR-350F (Mr. R. J. Wasneski) (1)
NAIR-360B (Mr. B. A. Zempolich) (1)
NAIR-360 (Mr. C. Thomas) (1)
NAIR-52022B1 (Mr. G. B. Cudd) (1)
NAIR-533DX (Mr. R. S. Entner) (1)
PMA-263 (CAPT W. M. Locke) (1)

Naval Avionics Facility
Indianapolis, Ind 46218

NAFI-072.9 (Mr. R. H. Huss) (1)
NAFI-D072 (Mr. W. Bridges) (1)
NAFI-D824 (Mr. C. W. Hagen) (1)
NAFI-D824 (Mr. J. Carr) (1)

NAFI-D900 (Mr. R. Barnett) (1)
NAFI-D924 (Mr. G. Forsee) (1)

Naval Electronic Systems Command
Washington, D. C. 20360
ELEX-304 (Mr. J. Cauffman) (1)

Naval Material Command
Washington, D. C. 20362
NMAT-0321 (Mr. S. Jacobson) (1)
NMAT-0321 (Mr. C. Lyons) (1)

Naval Ocean Systems Center
San Diego, CA 92152
NOSC-19 (Mr. S. Maynard) (1)
NOSC-722 (Ms. N. S. Mathis) (1)
NOSC-8222 (Mr. D. Wilcox) (1)
NOSC-9102 (Mr. W. Dejka) (1)
NOSC-923 (Mr. E. C. Urban) (1)
NOSC-923 (Mr. J. F. Poulson) (1)
NOSC-923 (Mr. E. S. Holland) (1)
NOSC-9232 (Dr. R. Martinez) (1)
NOSC-9232 (Mr. R. D. Peterson) (1)
NOSC-923 (Mr. A. Johnson) (1)

Naval Post Graduate School
Monterey, CA 93940
Dr. T. F. Tao 62TV

Naval Sea Systems Command
Washington, D. C. 20362
NSEA-03132 (Mr. R. Cuddy) (1)

NSEA-0341 (Mr. T. Tasaka) (1)
NSEA-393M2 (CDR J. Miltonberger) (1)
PMS-406 (CAPT M. T. Greeley) (1)

Naval Surface Weapons Center
Dahlgren Laboratory
Dahlgren, VA 22448
DF-34 (Mr. R. Holden) (6)
DF-34 (Mr. R. Dorsey) (1)
DF-14 (Mr. R. Wehman) (6)

Naval Surface Weapons Center
White Oak Laboratory
Silver Spring, MD 20910
WA-32 (Mr. A. Kolodzinski) (1)

Naval Weapons Center
China Lake, CA 93555
NWC-01 (Mr. R. M. Hillyer) (1)
NWC-015 (Dr. R. Cartwright) (1)
NWC-033 (Mr. C. Neal) (1)
NWC-395 (Mr. W. G. Hueber) (1)
NWC-3130 (Mr. L. Lakin) (1)
NWC-3132 (Mr. R. Hawkins) (1)

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217
ONR 212 (L/CDR W. Savage) (6)
ONR 230 (Mr. A. White) (1)
ONR 102IP (6)
ONR 221 (Mr. J. Trimble) (1)

Office of Naval Research Branch Office
495 Summer Street
Boston, Mass 02210 (1)

U.S. Army Electronics Command
Fort Monmouth, N. J. 07703
NL-BP (Mr. D. Haratz) (1)

U.S. Army Missile R&D Command
Redstone Arsenal, Ala 35809
DRDMI-TG (Mr. J. B. Huff) (1)
DRDMI-TGG (Mr. D. Ciliax) (1)
DRDMI-TE (Mr. D. Holter) (1)
DRDMI-EA (Mr. C. Riley) (1)
DRCPM-PE-X (Mr. W. Jann) (1)
DRCPM-MD (Mr. E. Wood) (1)

U.S. Naval Research Laboratory
Washington, D. C. 20375
NRL 2627 (6)
NRL 5216 (Mr. L. Palkuti) (1)
NRL 5260 (Dr. D. Barbe) (1)